

Advanced RISC Machine (ARM)

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Advanced RISC Machine (ARM) (originally Acorn RISC Machine) is a family of reduced instruction set computing (RISC) architectures for computer processors, configured for various environments. Arm Holdings develops the architecture and licenses it to other companies, who design their own products that implement one of those architectures—including systems-on-chips (SoC) and systems-on-modules (SoM) that incorporate memory, interfaces, radios, etc. It also designs cores that implement this instruction set and licenses these designs to a number of companies that incorporate those core designs into their own products.

Processors that have a RISC architecture typically require fewer transistors than those with a complex instruction set computing (CISC) architecture (such as the x86 processors found in most personal computers), which improves cost, power consumption, and heat dissipation. These characteristics are desirable for light, portable, battery-powered devices—including smartphones, laptops and tablet computers, and other embedded systems — while also useful, to some degree, for servers, and for desktops, where ARM chips were first used. Now, since ARM is a power-efficient solution, it is used in all kinds of devices up to the fastest supercomputer. A few other supercomputers are, however, more power-efficient, while none is without help of accelerators (heterogeneous computing), most often Nvidia GPUs.

Source: https://en.wikipedia.org/wiki/ARM_architecture

Datasheet	
Developer/Designer	Arm Holdings
Bits	32-bit, 64-bit
Introduced	1985
Design	RISC
Type	Register-Register
Encoding	AArch64/A64 ARM 64/32-bit and AArch32/A32 use 32-bit instructions, T32 (Thumb-2) uses mixed 16- and 32-bit instructions; ARMv7 user-space compatibility. ARM 32-bit (Cortex) and ARM 32-bit (legacy) 32-bit, except Thumb-2 extensions use mixed 16- and 32-bit instructions.
Endianness	Bi
Official Website	https://www.arm.com/

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