

SuperH (SH)

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SuperH (SH) is a 32-bit reduced instruction set computing (RISC) instruction set architecture (ISA) developed by Hitachi and currently produced by Renesas. It is implemented by microcontrollers and microprocessors for embedded systems.

At the time of introduction, SH2 was notable for having fixed-length 16-bit instructions in spite of its 32-bit architecture. This was a novel approach: at the time RISC processors instruction width was always dictated by architecture width. In other words, 32-bit RISC processors always used fixed 32-bit instructions.

Later the idea of what is now called compressed instruction set[citation needed] was adopted by other companies, most notable example being ARM that licensed relevant SuperH patents to create Thumb instruction set.

As of 2015, many of the original patents for the SuperH architecture are expiring and the SH2 CPU has been reimplemented as open source hardware under the name J2.

Source: https://en.wikipedia.org/wiki/SuperH#J_Core

Datasheet	
Developer	Hitachi
Bits	32-bit, 64-bit
Introduced	1990's
Design	RISC
Type	
Encoding	SH2: 16-bit instructions; SH2A and newer: mixed 16- and 32-bit instructions
Endianness	BI
Extensions	
Official Website	

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Last update: 2020/12/04 15:21

